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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/063,737	05/09/2002	Jimmy Hsu	8727-US-PA	6244

31561 7590 09/21/2004

JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE
7 FLOOR-1, NO. 100
ROOSEVELT ROAD, SECTION 2
TAIPEI, 100
TAIWAN

EXAMINER	
BOWERS, BRANDON	
ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 09/21/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/063,737	HSU, JIMMY	
	Examiner	Art Unit	
	Brandon W Bowers	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 September 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *16-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *16-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 September 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination

Applicant amended claim 16 and Figure 5 to show the new limitation "wherein the voltage reference signal trace is wider than the other signal traces" and states in the paper received 13 September 2004 that this feature is described in paragraph 0034 of the specification. However, the support for the claim limitation is found in paragraph 37.

Drawings

The drawings are objected to because new limitation added to the claims "wherein the voltage reference signal trace is wider than the other signal traces" and described in the specification in paragraph 0037 state that the second voltage reference signal trace (226) is wider, not the first voltage reference signal trace (204a). Figures 6 and 7 should be corrected to show this feature and figure 5 should be returned to it's original state. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the

drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 16-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sharma et al, US Patent No. 5,990,547 in view of Brooks et al., US Patent No. 6,326,244.

In reference to claim 16, Sharma teaches a multi-layered substrate having a voltage reference signal circuit layout therein (Figure 1 and column 3 line 53 – column 4 line 19) comprising at least one signal layer having a plurality of signal traces (column 3, lines 54-55), a non-signaling layer having a voltage reference signal trace (column 3, lines 55-56), and a conductive plane between the signal layer and the non-signal layer (column 3, lines1-13). Sharma does not teach wherein the voltage reference signal trace is wider than the other signal traces. Brooks teaches wherein voltage reference

signal trace is wider than the other signal traces (column 8, lines 52-67). Accordingly, it would have been obvious for one skilled in the art at the time of invention to incorporate the teachings of Sharma and Brooks to make a multi-layered substrate having all the limitations of claim 16 because it would reduce the self inductance associated with closely-adjacent, elongated traces by reducing the magnetic flux caused by oppositely directed currents flowing in the traces and the voltage reference signal trace.

In reference to claim 17, Sharma teaches wherein the non-signaling layer includes at least one power plane (column 3, lines 53-57).

In reference to claim 18, Sharma teaches wherein the non-signaling layer includes at least one ground layer plane (column 3, lines 53-57).

In reference to claim 19, Sharma teaches wherein the non-signaling layer includes at least one power plane and a plurality of signal traces (column 3, lines 57-column 4, line 19).

In reference to claim 20, Sharma teaches wherein the non-signaling layer includes at least one ground layer plane and a plurality of signal traces (column 3, lines 57-column 4, line 19).

In reference to claim 21, Sharma teaches wherein the conductive plane includes a ground plane (column 3, lines1-13 and 55-57).

In reference to claim 22, Sharma teaches wherein the conductive plane includes a power plane (column 3, lines1-13 and 55-57).

Claims 16-22 are rejected under 35 U.S.C. 102(b) as being anticipated by Honsinger et al., US Patent No. 5,500,804 in view of Brooks et al., US Patent No. 6,326,244.

In reference to claim 16, Honsinger teaches a multi-layered substrate having a voltage reference signal circuit layout therein comprising at least one signal layer having a plurality of signal traces, a non-signaling layer having a voltage reference signal trace, and a conductive plane between the signal layer and the non-signal layer (Figure 1 and column 3 line 64 – column 4 line 33). Honsinger does not teach wherein the voltage reference signal trace is wider than the other signal traces. Brooks teaches wherein voltage reference signal trace is wider than the other signal traces (column 8, lines 52-67). Accordingly, it would have been obvious for one skilled in the art at the time of invention to incorporate the teachings of Sharma and Brooks to make a multi-layered substrate having all the limitations of claim 16 because it would reduce the self inductance associated with closely-adjacent, elongated traces by reducing the magnetic flux caused by oppositely directed currents flowing in the traces and the voltage reference signal trace.

In reference to claim 17, Honsinger teaches wherein the non-signaling layer includes at least one power plane (Figure 1 and column 3 line 64 – column 4 line 33).

In reference to claim 18, Honsinger teaches wherein the non-signaling layer includes at least one ground layer plane (Figure 1 and column 3 line 64 – column 4 line 33).

In reference to claim 19, Honsinger teaches wherein the non-signaling layer includes at least one power plane and a plurality of signal traces (Figure 1 and column 3 line 64 – column 4 line 33).

In reference to claim 20, Honsinger teaches wherein the non-signaling layer includes at least one ground layer plane and a plurality of signal traces (Figure 1 and column 3 line 64 – column 4 line 33).

In reference to claim 21, Honsinger teaches wherein the conductive plane includes a ground plane (Figure 1 and column 3 line 64 – column 4 line 33).

In reference to claim 22, Honsinger teaches wherein the conductive plane includes a power plane (Figure 1 and column 3 line 64 – column 4 line 33).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brandon W Bowers whose telephone number is (571)272-1888. The examiner can normally be reached on 8:30 am until 5:00 pm Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on (571)272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

BWB

LEIGH M. GARBOWSKI
PRIMARY EXAMINER